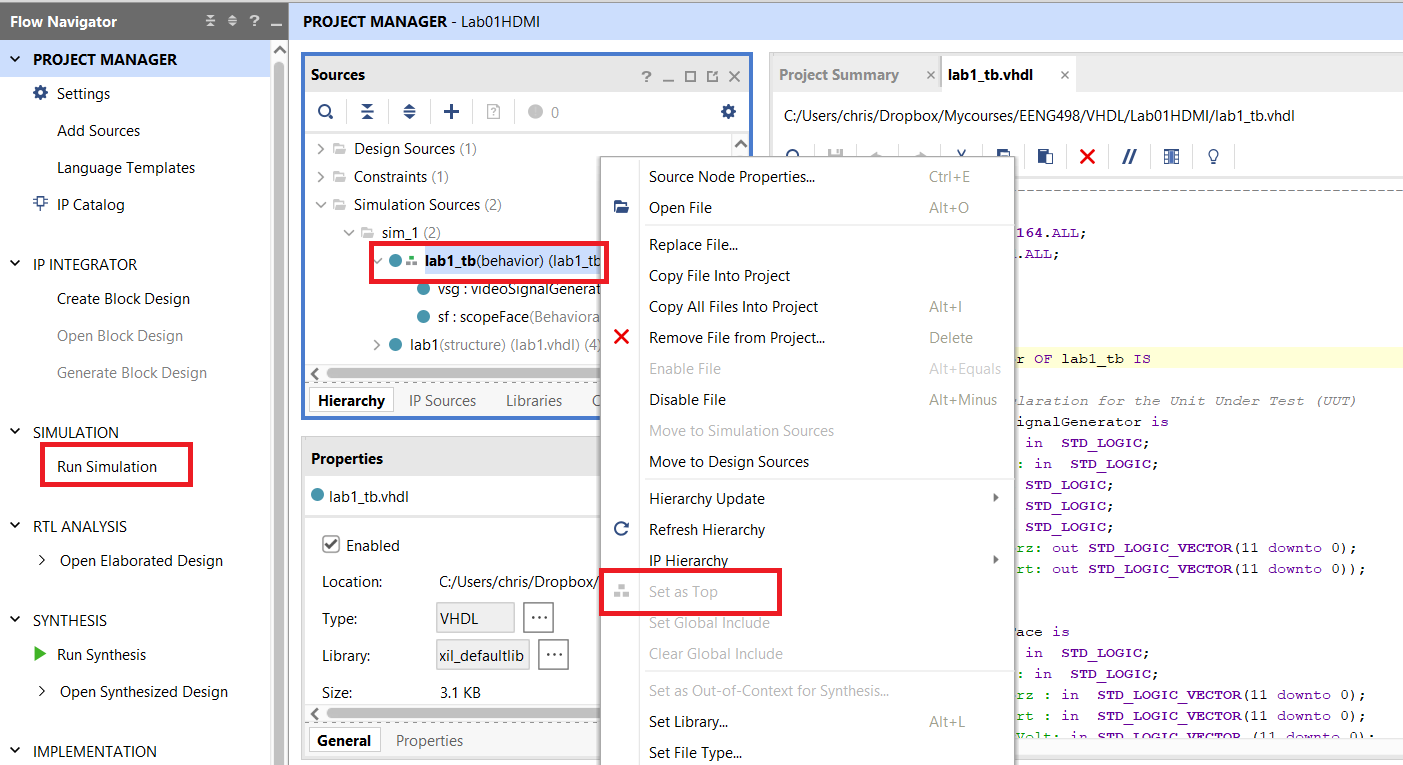
1. Start your simulation, make sure the testbench is the top-level file. To do this right click on the testbench file and select “Set as Top”. Then click on Run Simulation -> Run Behavioral.



2. Edit the TCL file to contain the signals you want in the testbench timing diagram



3. In the TCL console area

* Change directory to the TCL file by typing “cd <directory>” at the TCL prompt.
* Delete all the existing traces in the timing diagram. Click on name and then press “Del” key
* Execute the TCL file from the TCL prompt by typing “source <TCL filename>”.

